AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-6.   (canceled).

7.   (currently amended): <u>A method for detecting unstable clock-domain crossings in a design of an integrated circuit (IC), comprising:</u>

<u>determining clock-domain crossings in the design;</u>

<u>making a stability determination for a clock-domain crossing lacking a structural synchronization cell determined in the design</u><s>The method of claim 1</s>,

wherein the stability determination is made based on satisfaction of a stability function.

8.   (original):   The method of claim 7, wherein the stability function determines whether a first register and a second register change data simultaneously.

9.   (original):   The method of claim 8, wherein the stability function is dissatisfied when the first register and the second register change data simultaneously.

10.   (currently amended): The method of claim 9, wherein the first register belongs to a first clock domain and the second register belongs to a second clock domain, and the first <u>clock-domain</u> and <u>the</u> second clock <s>domains</s> <u>domain</u> are part of the <u>determined clock-domain</u> crossing.

11.   (currently amended): The method of claim ~~1~~7, wherein the stability determination

is performed using at least one of model checking and bounded model checking (BMC).

12-21. (canceled).

22.   (currently amended): A computer program product, including a computer

readable medium with computer instructions, for use by a computer to perform operations for

detecting unstable clock-domain crossings in a design of an integrated circuit (IC), the operations

comprising:

determining clock-domain crossings in the design;

making a stability determination for a clock-domain crossing lacking a structural

synchronization cell determined in the design, ~~The computer program product of claim 16~~,

wherein the stability determination is made based on satisfaction of a stability function.

23.   (original):   The computer program product of claim 22, wherein the stability

function determines whether a first register and a second register change data simultaneously.

24.   (original):   The computer program product of claim 23, wherein the stability

function is dissatisfied when the first register and the second register change data simultaneously.

25.   (currently amended): The computer program product of claim 24, wherein the

first register belongs to a first clock domain and the second register belongs to a second clock

domain, and the first clock-domain and the second clock ~~domains~~-domain are part of the

determined clock-domain crossing.

26. (currently amended): The computer program product of claim ~~16~~22, wherein the stability determination is performed using at least one of model checking and bounded model checking (BMC).

27-36. (canceled).

37. (currently amended): A computer system, adapted to implement a method for detecting unstable clock-domain crossings in a design of an integrated circuit (IC), comprising:

a processor; and,

a memory including software instructions adapted to enable the computer system to perform the operations of:

determining clock-domain crossings in the design;

making a stability determination for the clock-domain crossing lacking a structural synchronization cell determined in the design, and

~~The computer system of claim 31,~~ wherein the stability determination is made based on satisfaction of a stability function.

38. (original): The computer system of claim 37, wherein the stability function determines whether a first register and a second register change data simultaneously.

39. (original): The computer system of claim 38, wherein the stability function is dissatisfied when the first register and the second register change data simultaneously.

40.   (currently amended): The computer system of claim 39, wherein the first register belongs to a first clock domain and the second register belongs to a second clock domain, and the first clock-domain and the second clock ~~domains~~ domain are part of the determined clock-domain crossing.

41.   (currently amended): The computer system of claim 37~~31~~, wherein the stability determination is performed using at least one of model checking and bounded model checking (BMC).

42-45. (canceled).